REMARKS

Claims 1-12 remain in the application for consideration by the Examiner.

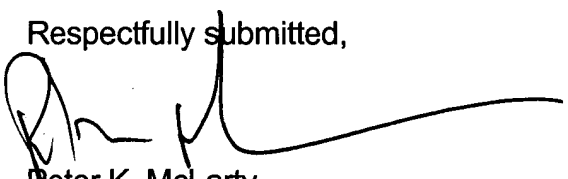
An early and favorable action is respectfully requested.

Should the Examiner have any comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



Peter K. McLarty
Attorney for Applicants
Reg. No. 44,923

Texas Instruments Incorporated
Mail Station 3999
P.O. Box 655474
Dallas, TX 75265
Phone: (972) 917-4258

Version with Markings to Show Changes Made

1(Amended). A method for forming a dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer of a first thickness over said silicon substrate;

forming a first etch stop layer over said first dielectric layer;

forming a second dielectric layer of a second thickness over said first dielectric layer;

forming an anti-reflective coating layer over said second dielectric layer;

etching a first trench [to a first depth] in said second dielectric layer [wherein the first depth is greater than the thickness of said second dielectric layer]; and

simultaneously etching a second trench to a [second] first depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the

[second] first depth is approximately equal to the second thickness [and the first depth is approximately equal to the first thickness].

7(Amended). A method for forming a copper filled dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer of a first thickness over said silicon substrate;

forming a first etch stop layer over said first dielectric layer;

forming a second dielectric layer of a second thickness over said first dielectric layer;

forming a silicon oxynitride anti-reflective coating layer over said second dielectric layer;

etching a first trench to a first depth in said second dielectric layer and said first dielectric layer wherein the first depth is greater than the thickness of said second dielectric layer; and

simultaneously etching a second trench to a second depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the second depth is approximately equal to the second thickness [and the first depth is approximately equal to the first thickness].

8 (Amended). The method of claim [1] 7 wherein said silicon nitride anti-reflective coating layer comprises 30 to 50 atomic percent of silicon, 20 to 50 atomic percent of oxygen, 2 to 17 atomic percent of nitrogen, and 7 to 35 atomic percent of hydrogen.

9 (Amended). The method of claim [1] 7 wherein first and second etch stop layers are formed with material selected from the group consisting of silicon carbide and silicon nitride.

10 (Amended). The method of claim [1] 7 wherein said first dielectric layer is FSG.

11 (Amended). The method of claim [1] 7 wherein said second dielectric layer is FSG.

12 (Amended). The method of claim [1] 7 further comprising:

forming a liner film in said first trench and said second trench; and

forming a contiguous copper layer in said first trench and said second trench.